WHAT IS CLAIMED IS:

1. A double-data rate (DDR) bus system for use in a host-daughtercard interface that is pin compatible with a legacy interface used to interface a legacy daughtercard with the host, with legacy interface including a parallel port utilized by the host to write values to registers on the daughtercards, with the parallel port utilizing a subset of pins on a host-daughtercard connector, with the bus system comprising:

a daughtercard termination logic block, coupled to the subset of pins previously used for the parallel port that redefines the subset of pins as a set of receive pins, a receive control pin, a receive clock pin, a set of transmit pins, a control pin, and a transmit clock pin;

a host termination logic block, coupled to the subset of pins previously used for the parallel port that redefines the subset of pins as a set of receive pins, a receive control pin, a receive clock pin, a set of transmit pins, a transmit control pin, and a transmit clock pin;

where the daughtercard termination logic implements DMA transfers between memory or registers on the daughtercard and host memory, and where packet data is transferred using generic data frames, where control is asserted utilizing control frames, and where a control signal is asserted on the control pin to indicate control frames;

where the host termination logic utilizes read and write frames to implement the function of the legacy parallel port to read and write data to daughtercard registers, where packet data is transferred using generic data frames, where DMA data is transferred using DMA data frames, where control is asserted utilizing control frames, and where a control signal is asserted on the control pin to indicate control frames.

2. The system of claim 1 where:

the daughtercard termination logic utilizes an interrupt control frame to interrupt a processor on the host.

3. The system of claim 1 where:

the host interface and daughtercard interface implement flow control by inserting idle control bytes in the middle of a data frame to prevent data frames from underrunning.

4. The system of claim 1 where:

host memory includes buffer descriptors with an address field having a specified number of bytes; and

where the daughtercard includes an extension register holding bits which are concatenated with an address held in a buffer descriptor to extend the address held in the buffer descriptor.

5. The system of claim 1 where the legacy interface includes a serial peripheral interface coupled to a second subset of pins on host-daughtercard connector, and where:

the daughtercard includes a non-volatile memory for storing daughtercard identification information including information indicating whether the daughter card implements the legacy interface or the DDR bus; and where:

the host termination logic block utilizes the legacy serial peripheral interface to read non-volatile memory on the daughtercard and configures the first set of pins as the legacy parallel port if the daughtercard identification indicates that the daughtercard supports the legacy interface or configures the first set of pins as the DDR bus if the daughtercard identification indicates that the daughtercard supports the DDR bus interface.

6. A bus system interface comprising:

a host, having a host bus interface that is pin compatible with a legacy bus defining a parallel port and a serial bus, with the host bus interface including serial bus logic that determines whether a connected daughtercard is a legacy daughtercard or a high-speed daughtercard and the host bus interface including DDR bus logic that redefines a set of the pins to implement a double-data rate (DDR) bus when a high-speed daughtercard is detected; and

a high-speed daughtercard, having a daughtercard bus interface implementing a DDR bus and a serial bus, and including identification information that allows the host bus interface to determine whether a high-speed daughtercard is connected.

7. A bus system comprising:

a host that is pin compatible with a legacy bus that defines a parallel port and a serial bus, with the host including:

means for interfacing with the serial bus;

means, coupled to the means for interfacing with the serial bus, for determining whether a connected daughtercard is a legacy daughtercard or a high-speed daughtercard;

means for redefining a set of the pins to implement a double-data rate (DDR) bus when a high-speed daughtercard is detected; and

a high speed daughtercard including:

means for implementing the DDR bus and the serial bus; and

means for providing identification information that allows the host bus interface to determine whether a high-speed daughtercard is connected.

8. The system of claim 7 further comprising:

at the host:

means for utilizing read and write transactions to implement the functions of the parallel port.

9. The system of claim 7 further comprising:

at the daughtercard:

means for utilizing an interrupt control frame to interrupt the host.

10. The system of claim 2 where the host includes a memory holding buffer descriptors with an address field having a specified number of bytes, the system further comprising:

at the daughtercard:

means for extending the address held in the buffer descriptor using bits held at the daughtercard.

11. A bus system interface comprising:

a host, having a host bus interface that is pin compatible with a legacy bus defining a parallel port and a serial bus, with the host bus interface including serial bus logic that determines whether a connected daughtercard is a legacy daughtercard or a high-speed daughtercard and the host bus interface including DDR bus logic that redefines a set of the pins to implement a double-data rate (DDR) bus when a high-speed daughtercard is detected.